REMARKS

Applicant respectfully requests that the Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this amendment presents claims in better form for consideration on appeal. Applicant submits that thus there is a good and sufficient reason why this amendment is necessary, why this amendment was not earlier presented, and why this amendment should be admitted now. Furthermore, applicant believes that consideration of this amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1-5, 7, 8, 12, and 14-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy et al. ("Levy"). This rejection is a new grounds or rejection, which was first presented in the Final Office Action mailed June 2, 2000.

Claims 6, 9, 10, 11, and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Levy. This rejection is also a new grounds of rejection, which was first presented in the Final Office Action mailed June 2, 2000.

Claims 1-17 are pending.

Claims 1, 2, 6, 8, 9, 14, and 17 have been amended in this amendment. No new claims have been added. Applicant respectfully submits that no new matter has been introduced by the amendments made herein.

35 U.S.C. § 102(b) Rejection

The Examiner has rejected claims 1-5, 7, 8, 12, and 14-17 under 35 U.S.C. § 102(b) as being anticipated by Levy. In particular, the Examiner states:

> Regarding claims 1, 2, and 17, Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first memory transaction in a first format from a first memory bus (memory bus 40) and converts the first memory transaction into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

(pp. 2-3 Office Action 6/2/00).

Applicant respectfully submits that claim 1 is not anticipated by Levy. To anticipate claim 1, Levy must disclose each and every limitation of claim 1. Claim 1 includes the limitations of:

> A memory module, comprising:
> a plurality of memory devices; and
> a memory module controller to receive a first memory transaction in a first format from a first memory bus, and to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

(Claim 1)(emphasis added).

Levy, however, fails to disclose a memory module controller to receive a first memory transaction in a first format from a first memory bus, and to convert the first memory transaction into a second memory transaction in a second format for the plurality

of memory devices as recited in claim 1. Levy further fails to disclose that the second format of the second memory transaction is different form the first format of the first memory transaction as recited in claim 1.

Levy, in Figure 1, discloses a memory module 30 coupled to associative memory 24. memory module 30 includes a memory transceiver 41 and memory control and timing circuit 42 coupled to low and high stacks 44 and 45, respectively. The Examiner associates memory transceiver 41 and memory control and timing circuit 42 of Levy with the claimed memory module controller as recited in claim 1.

The memory transceiver 41 and memory control and timing 42, however, are not related to converting a memory transaction in a first format into a memory transaction in a second format. In particular, Levy discloses that:

> . . . During a writing operation, the associative memory 24 transmits BYTE MASK signals (FIG. 5) to the memory control and timing circuit 42 thereby to select one byte or some combination of bytes in the addressed location.
>
> Still referring to FIGS. 1 and 5, the associative memory 24 transmits an ADDRESS PARITY signal which is based upon the value of the address and various control signals that initiate a memory cycle and also data signals if data is being transferred from the associative memory 24. Next the associative memory 24 transmits a START signal that enables the memory control and timing circuit 42 (FIG. 1) to initiate a memory cycle. The circuit 42 transmits back to the associative memory 24 an ACKNOWLEDGE signal that terminates the address and control signals and the BYTE MASK, parity, data and START signals. During a reading memory cycle, the associative memory 24 can initiate another memory cycle with another memory until after the ACKNOWLEDGE signal is terminated.

Thus, Levy teaches that memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, Levy

does not teach that the memory control and timing circuit 42 converts a first memory transaction into a second memory transaction.

Therefore, for the above reasons, claim 1 is not anticipated by Levy. Given that claims 2-16 depend directly or indirectly on claim 1, claims 2-16 are not anticipated by Levy.

Applicant respectfully submits that claim 17 is not anticipated by Levy. To anticipate claim 17, levy must disclose each and every limitation of claim 17. Claim 17 includes the limitations of:

> A memory module, comprising:
> a plurality of memory devices; and
> a memory module controller coupled to the plurality of memory devices, the memory module controller to receive a first memory transaction in a first format from a memory bus, and to convert the first memory transaction into a second memory transaction in a second format, and to provide the second memory transaction in the second format to at least one of the plurality of memory devices.

(Claim 17)(emphasis added).

Levy, however, fails to disclose a memory module having a memory module controller coupled to the plurality of memory devices and to receive a first memory transaction in a first format from a memory bus, and to convert the first memory transaction into a second memory transaction in a second format, and to provide the second memory transaction in the second format to at least one of the plurality of memory devices as recited in claim 17.

As noted above, Levy does not teach converting memory transactions. Therefore for the above reasons, claim 17 is not anticipated by Levy.

35 U.S.C. § 103(a) Rejection

The Examiner has rejected claims 6, 9, 10, 11, and 13 under 35 U.S.C. § 103(a) as being unpatentable over Levy. In particular, the Examiner states:

> Regarding claim 6, Levy does not teach that his memory buses operate at different rates, however it would have been obvious to one skilled in the art at the time of the invention to operate them at different rates since they carry different signals and have different lengths, virtually ensuring that the maximum data rate of each one would be different.
>
> Regarding claim 9, Levy shows separate address and data lines for both his first and second memory buses. He does not teach that his first memory bus carries time-multiplexed data and address information as claimed, however it would have been obvious to one skilled in the art to time-multiplex the first address bus to save signal lines and their associated cost and space.
>
> Regarding claims 10, 11, and 13, Levy does not teach that his memory modules have the claimed characteristics, however it would have been obvious to the skilled artisan at the time of the invention to implement Levy's memory modules as SIMMs, DIMMs, or nonvolatile memory devices, as appropriate, depending on design considerations, since all three types of devices were well-known to the artisan.

It is respectfully submitted that the Examiner relies on impermissible hindsight to render claims 6, 9, 10, 11, and 13 obvious. Nowhere in Levy does it disclose or suggest memory buses operating at different rates, carrying time-multiplexed data, a DIMM memory module, a SIMM memory module, and nonvolatile memory devices as recited in claims 6, 9, 10, 11, and 13, respectively.

Furthermore, because Levy fails to disclose the limitations of claim 1 and claims 6, 9, 10, 11, and 13 are dependent directly on claim 1, claims 6, 9, 10, 11, and 13 are patentable over Levy.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable §102(b) and §103(a) rejections have been overcome.

Accordingly, applicant respectfully requests that claims 1-17 be found in condition of allowance.

If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: August 15, 2000

Sang Hui Michael Kim
Reg. No. 40,450

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300